DDR2 VLP Registered DIMM (RDIMM)

MT18HVF12872(P) – 1GB

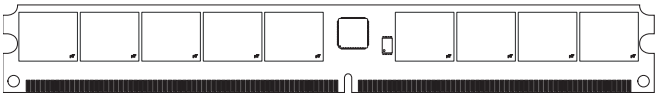
For the latest data sheet and for component data sheets, refer to Micron's Web site: www.micron.com/products/ddr2

Features

- Supports 95°C with double refresh
- Fits with the ATCA form factor
- 240-pin, registered dual in-line memory module
- Fast data transfer rates: PC2-3200, PC2-4200, or PC2-5300
- Supports ECC error detection and correction
- V_{DD} = $V_{DD}Q$ = +1.8V
- V_{DDSPD} = +1.7V to +3.6V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Single rank
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts

Figure 1: 240-Pin VLP DIMM (MO-237)
Functionally equivelent to R/C "U" and "V"

Height: 17.9mm (0.705in)



Options	Marking
• Parity	P
• Package	
240-pin DIMM (lead-free)	Y
• Frequency/CAS latency[1]	
3.0ns @ CL = 5 (DDR2-667)[2]	-667
3.75ns @ CL = 4 (DDR2-533)	-53E
5.0ns @ CL = 3 (DDR2-400)	-40E
• PCB height	
17.9mm (1.18in)	

Notes: 1. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
2. Contact Micron for product availability.

Table 1: Addressing

	1GB
Refresh count	8K
Row address	16K (A0–A13)
Device bank address	4 (BA0, BA1)
Device page size per bank	1KB
Device configuration	512Mb (128 Meg x 4)
Column address	2K (A0–A9, A11)
Module rank address	1 (S0#)

Table 2: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 5	CL = 4	CL = 3			
-667	PC2-5300	667	533	–	15	15	55
-53E	PC2-4200	–	533	400	15	15	55
-40E	PC2-3200	–	400	400	15	15	55

Figure 2: Module Part Numbers

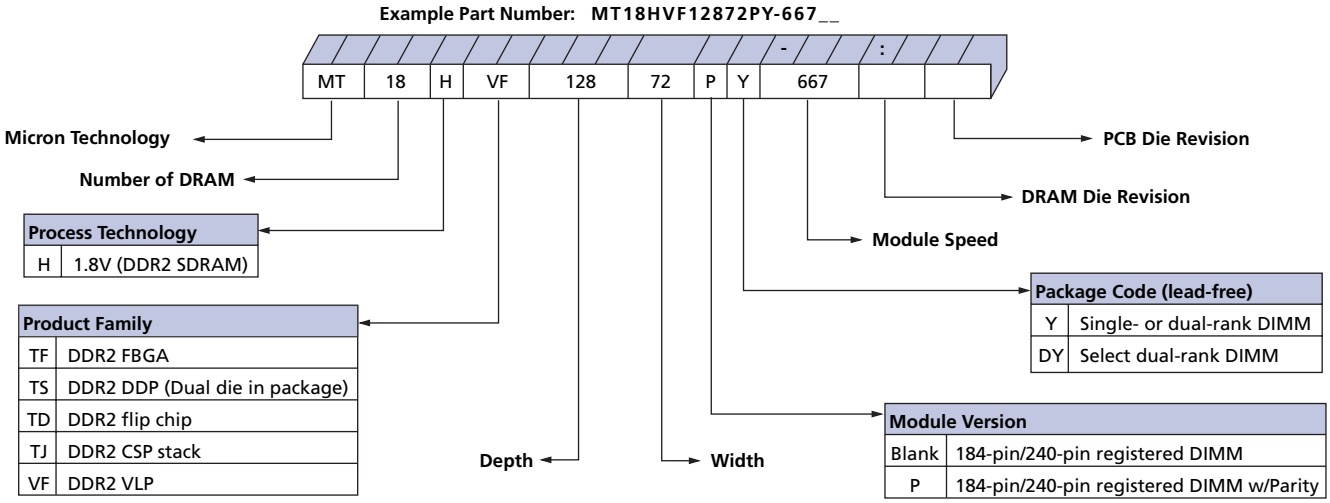


Table 3: Part Numbers and Timing (1GB – 128 Meg x 72)

Uses 512Mb (128 Meg x 4) – MT47H128M4 DDR2 SDRAM – www.micron.com/products/ddr2

Part Number	Industry Nomenclature	Module Bandwidth	Clock Cycle Time (ns)	Data Rate (MT/s)	Latency (CL - ^{t}RCD - ^{t}RP)	DRAM Speed Grade
MT18HVF12872(P)Y-667__	PC2-5300	5.3 GB/s	3.0	667	5-5-5	-3
MT18HVF12872(P)Y-53E__	PC2-4200	4.2 GB/s	3.75	533	4-4-4	-37E
MT18HVF12872(P)Y-40E__	PC2-3200	3.2 GB/s	5.0	400	3-3-3	-5E

Notes: 1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18HVF12872PY-667C2.

Pin Assignments and Descriptions

Table 4: Pin Assignment

240-Pin RDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	31	DQ19	61	A4	91	VSS
2	VSS	32	VSS	62	VDDQ	92	DQS5#
3	DQ0	33	DQ24	63	A2	93	DQS5
4	DQ1	34	DQ25	64	VDD	94	VSS
5	VSS	35	VSS	65	VSS	95	DQ42
6	DQS0#	36	DQS3#	66	VSS	96	DQ43
7	DQS0	37	DQS3	67	VDD	97	VSS
8	VSS	38	VSS	68	PAR_IN	98	DQ48
9	DQ2	39	DQ26	69	VDD	99	DQ49
10	DQ3	40	DQ27	70	A10/AP	100	VSS
11	VSS	41	VSS	71	BA0	101	SA2
12	DQ8	42	CB0	72	VDDQ	102	NC
13	DQ9	43	CB1	73	WE#	103	VSS
14	VSS	44	VSS	74	CAS#	104	DQS6#
15	DQS1#	45	DQS8#	75	VDDQ	105	DQS6
16	DQS1	46	DQS8	76	S1#	106	VSS
17	VSS	47	VSS	77	ODT1	107	DQ50
18	RESET#	48	CB2	78	VDDQ	108	DQ51
19	NC	49	CB3	79	VSS	109	VSS
20	VSS	50	VSS	80	DQ32	110	DQ56
21	DQ10	51	VDDQ	81	DQ33	111	DQ57
22	DQ11	52	CKE0	82	VSS	112	VSS
23	VSS	53	VDD	83	DQS4#	113	DQS7#
24	DQ16	54	NC/BA2	84	DQS4	114	DQS7
25	DQ17	55	ERR_OUT	85	VSS	115	VSS
26	VSS	56	VDDQ	86	DQ34	116	DQ58
27	DQS2#	57	A11	87	DQ35	117	DQ59
28	DQS2	58	A7	88	VSS	118	VSS
29	VSS	59	VDD	89	DQ40	119	SDA
30	DQ18	60	A5	90	DQ41	120	SCL

240-Pin RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	VSS	151	VSS	181	VDDQ	211	DQS14
122	DQ4	152	DQ28	182	A3	212	DQS14#
123	DQ5	153	DQ29	183	A1	213	VSS
124	VSS	154	VSS	184	VDD	214	DQ46
125	DQS9	155	DQS12	185	CK0	215	DQ47
126	DQS9#	156	DQS12#	186	CK0#	216	VSS
127	VSS	157	VSS	187	VDD	217	DQ52
128	DQ6	158	DQ30	188	A0	218	DQ53
129	DQ7	159	DQ31	189	VDD	219	VSS
130	VSS	160	VSS	190	BA1	220	RFU
131	DQ12	161	CB4	191	VDDQ	221	RFU
132	DQ13	162	CB5	192	RAS#	222	VSS
133	VSS	163	VSS	193	S0#	223	DQS15
134	DQS10	164	DQS17	194	VDDQ	224	DQS15#
135	DQS10#	165	DQS17#	195	ODT0	225	VSS
136	VSS	166	VSS	196	NC/A13	226	DQ54
137	RFU	167	CB6	197	VDD	227	DQ55
138	RFU	168	CB7	198	VSS	228	VSS
139	VSS	169	VSS	199	DQ36	229	DQ60
140	DQ14	170	VDDQ	200	DQ37	230	DQ61
141	DQ15	171	CKE1	201	VSS	231	VSS
142	VSS	172	VDD	202	DQS13	232	DQS16
143	DQ20	173	NC	203	DQS13#	233	DQS16#
144	DQ21	174	NC	204	VSS	234	VSS
145	VSS	175	VDDQ	205	DQ38	235	DQ62
146	DQS11	176	A12	206	DQ39	236	DQ63
147	DQS11#	177	A9	207	VSS	237	VSS
148	VSS	178	VDD	208	DQ44	238	VDDSPD
149	DQ22	179	A8	209	DQ45	239	SA0
150	DQ23	180	A6	210	VSS	240	SA1

Table 5: Pin Descriptions

Refer to Table 4 on page 3 for more information

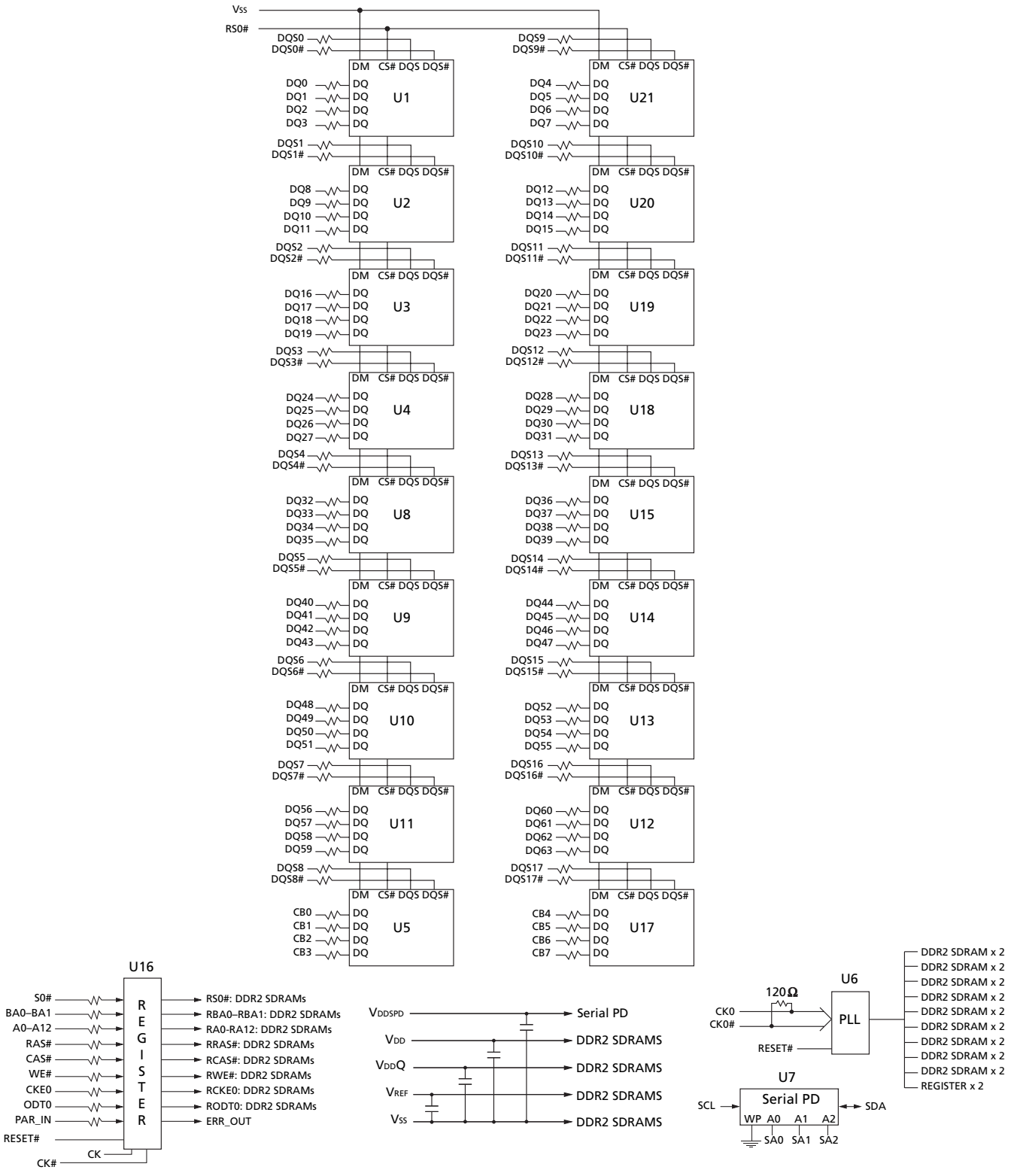
Symbol	Type	Source	Description
ODT0	Input (SSTL18)	Register	**On-die termination**: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
CK0, CK0#	Input (SSTL18)	PLL	**Clock**: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input (SSTL18)	Register	**Clock enable**: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM..
S0#	Input (SSTL18)	Register	**Chip select**: S# enables (registered LOW) and disables (registered HIGH) the command decoder.
RAS#, CAS#, WE#	Input (SSTL18)	Register	**Command inputs**: RAS#, CAS#, and WE# (along with S#) define the command being entered.
BA0, BA1	Input (SSTL18)	Register	**Bank address inputs**: BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
A0–A13	Input (SSTL18)	Register	**Address inputs**: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
PAR_IN	Input (SSTL18)	Register	Parity bit for the address and control bus.
SCL	Input	SPD	**Serial clock for presence-detect**: SCL is used to synchronize the presence-detect data transfer to and from the module.
SA0–SA2	Input	SPD	**Presence-detect address inputs**: These pins are used to configure the presence-detect device.
RESET#	Input (LVCMOS)	Register	Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.
DQS0–DQS17, DQS0#–DQS17#	I/O (SSTL18)	DRAM	**Data strobe**: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
DQ0–DQ63	I/O (SSTL18)	DRAM	**Data input/output**: Bidirectional data bus.
CB0–CB7	I/O (SSTL18)	DRAM	**Check bits**.
SDA	I/O	SPD	**Serial presence-detect data**: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
ERR_OUT	Output (open drain)	Register	Parity error found on the address and control bus.
VDD	Supply	DRAM, PLL, Register	**Power supply**: 1.8V ±0.1V.
VDDQ	Supply	DRAM	**DQ power supply**: 1.8V ±0.1V.

Table 5: Pin Descriptions (continued)
Refer to Table 4 on page 3 for more information

Symbol	Type	Source	Description
V_{REF}	Supply	DRAM, PLL, Register	SSTL_18 reference voltage.
V_{SS}	Supply	ALL	**Ground**.
V_{DDSPD}	Supply	SPD	**Serial EEPROM positive power supply**: +1.7V to +3.6V.
NC	–		**No connect**: These pins should be left unconnected.
RFU	–		Reserved for future use.

Functional Block Diagram

Figure 3: Functional Block Diagram



Unless otherwise noted, resister values a 22Ω per industry standard

General Description

Refer to the DDR2 component data sheets for complete functionality. For the 1GB RDIMM device, refer to the 512Mb (128 Meg x 4) component data sheet.

DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 1GB memory modules organized in x72 configuration. DRAM specifications require the refresh rate to double when T_{CASE} exceeds 85°C. This also includes the use of the high-temperature refresh option.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

PLL and Register Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The registers and PLL minimize system and clock loading. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Absolute Maximum DC Ratings

Parameter		Symbol	Min	Max	Units
VDD supply voltage relative to VSS		VDD	–1.0	2.3	V
VDDQ supply voltage relative to VSS		VDDQ	–0.5	2.3	V
VDDL supply voltage relative to VSS		VDDL	–0.5	2.3	V
Voltage on any pin relative to VSS		VIN, VOUT	–0.5	2.3	V
Storage temperature (2X refresh at 95°C)		T_{STG}	–55	100	°C
DDR2 SDRAM device operating temperature		T_{CASE}	0	95	°C
Input leakage current; Any input 0V ≤ VIN ≤ VDD; VREF input 0V ≤ VIN ≤ 0.95V; all other pins not under test = 0V	Command/address, RAS#, CAS#, WE# S#, CKE, CK, CK#, DM	II	–10	10	µA
Output leakage current; 0V ≤ VOUT ≤ VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	Ioz	–10	10	µA
VREF leakage current; VREF = valid VREF level		IVREF	–46	46	µA

Capacitance

At DDR2 data rates, Micron encourages designers to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

Table 7: DRAM Interface for DRAM I/O
DRAM (at each individual device pin)

Parameter	Symbol	Min	Max	Units
Input high (logic 1) voltage	VIH(DC)	VREF(DC) + 125	VDDQ + 300	mV
Input low (logic 0) voltage	VIL(DC)	–300	VREF(DC) - 125	mV
Input high (logic 1) voltage (-667 speed grade)	VIH(AC)	VREF(DC) + 200	–	mV
Input low(logic 0) voltage (-667 speed grade)	VIL(AC)	–	VREF(DC) - 200	mV
Input leakage current; any input 0V ≤ VIN ≤ VDD; all other pins not under test = 0V	Ii	–10	10	uA
Output leakage current; 0V ≤ VOUT ≤ VDDQ; DQ and ODT disabled	Ioz	–10	10	uA
Input/output capacitance	CIO	5.5	10.5	pF

IDD Specifications

Table 8: DDR2 IDD Specifications and Conditions – 1GB
Values shown for MT47H128M4 DDR2 SDRAM only and are computed from values specified in the 512Mb (128 Meg x 4) component data sheet

Parameter/Condition		Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0[a]	1,620	1,440	1,440	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1[a]	1,890	1,710	1,620	mA
Precharge power-down current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P[b]	126	126	126	mA
Precharge quiet standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q[b]	810	720	630	mA
Precharge standby current; All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N[b]	900	810	720	mA
Active power-down current; All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P[b]	630	540	450	mA
	Slow PDN exit MR[12] = 1		216	216	216	mA
Active standby current; All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N[b]	1,170	990	810	mA
Operating burst write current; All device banks open, Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W[a]	3,060	2,520	2,070	mA
Operating burst read current; All device banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R[a]	3,240	2,610	2,070	mA
Burst refresh current; ^{t}CK = ^{t}CK (IDD); REFRESH command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5[b]	3,240	3,060	2,970	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6[b]	126	126	126	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) -1 × ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during DESELECTs; Data bus inputs are switching		IDD7[a]	4,320	4,050	3,960	mA

Notes: 1. a = Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
2. b = Value calculated reflects all module ranks in this operating condition.

Registers

Table 9: Register (uses SSTU32865 devices)

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	$V_{IH(DC)}$	Address, Control, Command	SSTL_18	$V_{REF(DC)}$ +125	V_{DDQ} + 250	mV
DC low-level input voltage	$V_{IL(DC)}$	Address, Control, Command	SSTL_18	0	$V_{REF(DC)}$ - 125	mV
AC high-level input voltage	$V_{IH(AC)}$	Address, Control, Command	SSTL_18	$V_{REF(DC)}$ + 250	V_{DD}	mV
AC low-level input voltage	$V_{IL(AC)}$	Address, Control, Command	SSTL_18	0	$V_{REF(DC)}$ - 250	mV
Output high voltage	V_{OH}	Parity output	LVCMOS	1.2	–	mV
Output low voltage	V_{OL}	Parity output	LVCMOS	–	0.5	mV
Input current	I_I	All pins	V_I = V_{DDQ} or V_{SSQ}	–5	5	µA
Static standby	I_{DD}	All pins	RESET# = V_{SSQ} (I/O = 0)	–	100	µA
Static operating	I_{DD}	All pins	RESET# = V_{SSQ}; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$ I/O = 0	–	40mA	µA
Dynamic operating – clock tree	I_{DDD}	N/A	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I0 = 0; CK and CK# switching 50% duty cycle	–	Varies by mfr	µA
Dynamic operating (per each input)	I_{DDD}	N/A	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I0 = 0; CK and CK# switching 50% duty cycle; One data input switching at $^{t}CK/2$, 50% duty cycle	–	Varies by mfr	µA
Input capacitance (per device, per pin)	C_I	All inputs except RESET#	V_I = V_{REF} ±250mV; V_{DDQ} = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)		RESET#	V_I = V_{DDQ} or V_{SSQ}	–	Varies by mfr	pF

PLL

Table 10: PLL (uses a 97U877B device)

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V_{IH}	RESET#	LVCMOS	0.65 × V_{DD}	–	mV
DC low-level input voltage	V_{IL}	RESET#	LVCMOS	–	0.35 × V_{DD}	mV
Input voltage (limits)	V_{IN}	RESET#, CK, CK#		–0.3	$V_{DD}Q$ + 0.3	mV
DC high-level input voltage	V_{IH}	CK, CK#	Differential Input	0.65 × V_{DD}	–	mV
DC low-level input voltage	V_{IL}	CK, CK#	Differential Input	–	0.35 × V_{DD}	mV
Input differential-pair cross voltage	V_{IX}	CK, CK#	Differential Input	($V_{DD}Q$/2) - 0.15	($V_{DD}Q$/2) + 0.15	V
Input differential voltage	$V_{ID(DC)}$	CK, CK#	Differential Input	0.3	$V_{DD}Q$ + 0.4	V
Input differential voltage	$V_{ID(AC)}$	CK, CK#	Differential Input	0.6	$V_{DD}Q$ + 0.4	V
Input current	I_I	RESET#	V_I = $V_{DD}Q$ or $V_{SS}Q$	–10	10	µA
		CK, CK#	V_I = $V_{DD}Q$ or $V_{SS}Q$	–250	250	µA
Output disabled current	I_{ODL}		RESET# = $V_{SS}Q$; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$	100	–	µA
Static supply current	I_{DDLD}		CK = CK# = LOW	–	500	uA
Dynamic supply	I_{DD}	N/A	CK, CK# = 270 MHz, all outputs open (not connected to PCB)	–	300	mA
Input capacitance	C_{IN}	Each input	V_I = $V_{DD}Q$ or $V_{SS}Q$	2	3	pF

Table 11: PLL Clock Driver Timing Requirements and Switching Characteristics

Note: 1

Parameter	Symbol	0°C ≤ T_{OPR} ≤ +55°C, V_{DD} = +1.8V ±0.1V		Units
		Min	Max	
Stabilization time	^tL	–	15	µs
Input clock slew rate	^tLS_I	1.0	4	V/ns
SSC modulation frequency		30	33	kHZ
SSC clock input frequency deviation		0.0	–0.50	%
PLL loop bandwidth (-3dB from unity gain)		2.0	–	MHz

Notes: 1. Timing and switching specifications for the PLL listed above are critical for proper operation of the DDR2 SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this PLL is available in JEDEC Standard JESD82.

Serial Presence-Detect

Table 12: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 KHz	ICC_R	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 KHz	ICC_W	2	3	mA

Table 13: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
SDA and SCL fall time	^tF	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SDA and SCL rise time	^tR	–	0.3	µs	2
SCL clock frequency	^fSCL	–	400	KHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

Notes:
1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 14: Serial Presence-Detect Matrix
"1"/"0": serial data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT18HVF12872/ MT18HVF12872P
0	Number of SPD bytes used by Micron	128	80
1	Total number of bytes in SPD device	256	08
2	Fundamental memory type	DDR2 SDRAM	08
3	Number of row addresses on assembly	13, 14	0E
4	Number of column addresses on assembly	10	0B
5	DIMM height and module ranks	17.9mm, single rank	00
6	Module data width	72	48
7	Module data width (continued)	0	00
8	Module voltage interface levels	SSTL 1.8V	05
9	SDRAM cycle time, ^{t}CK (CL = MAX value, see byte 18)	-667 -53E -40E	30 3D 50
10	SDRAM access from clock, ^{t}AC (CL = MAX value, see byte 18)	-667 -53E -40E	45 50 60
11	Module configuration type	ECC/ECC and parity	02/06
12	Refresh rate/type	7.81µs/SELF	82
13	SDRAM device width (primary SDRAM)	4	04
14	Error-checking SDRAM data width	4	04
15	Reserved		00
16	Burst lengths supported	4, 8	0C
17	Number of banks on SDRAM device	4 or 8	08
18	CAS latencies supported	-667 (5, 4, 3) -53E/-40E (4, 3)	38 18
19	Module thickness		01
20	DDR2 DIMM type	Registered DIMM	01
21	SDRAM module attributes		04
22	SDRAM device attributes: weak driver (01) or 50Ω ODT (03)	-667 -53E/-40E	03 01
23	SDRAM cycle time, ^{t}CK, MAX CL - 1	-667 -53E/-40E	3D 50
24	SDRAM access from CK, ^{t}AC, MAX CL - 1	-667 -53E -40E	45 50 60
25	SDRAM cycle time, ^{t}CK, MAX CL - 2	-667 -53E/-40E(N/S)	50 00
26	SDRAM access from CK, ^{t}AC, MAX CL - 2	-667 -53E/-40E(N/S)	45 00
27	MIN row precharge time, ^{t}RP		3C
28	MIN row active to row active, ^{t}RRD		1E
29	MIN RAS# to CAS# delay, ^{t}RCD		3C
30	MIN RAS# pulse width, ^{t}RAS (see note 1)	-667/-53E -40E	2D 28
31	Module rank density	1GB	01

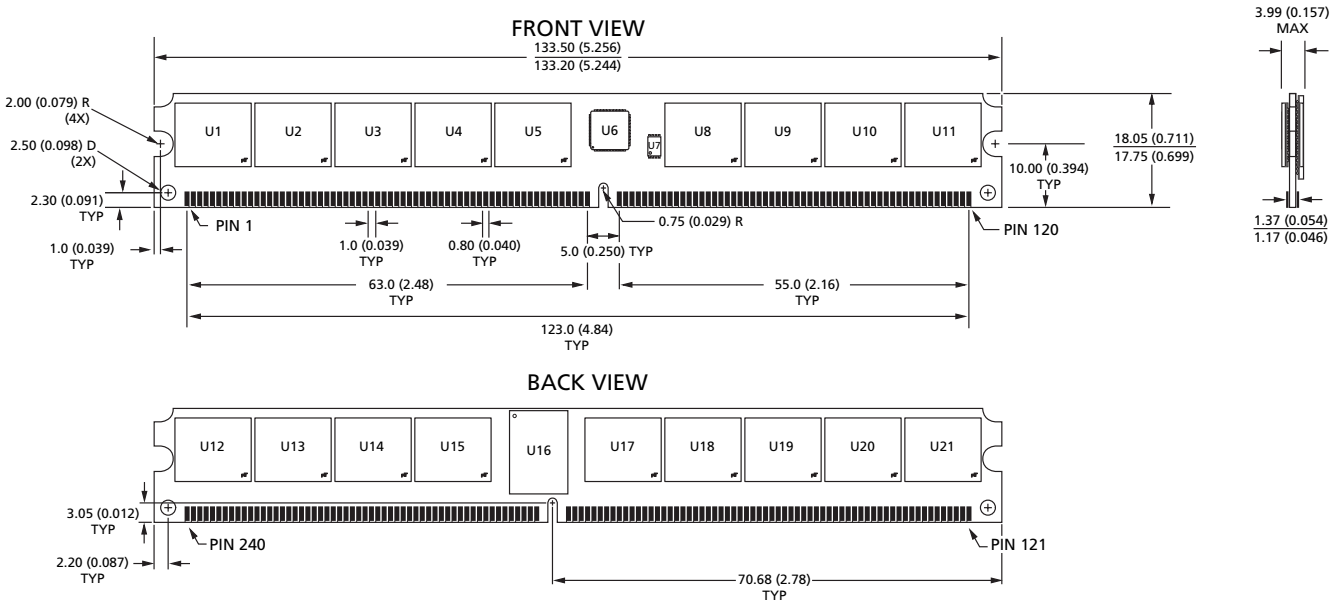
Table 14: Serial Presence-Detect Matrix (continued)
"1"/"0": serial data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT18HVF12872/ MT18HVF12872P
32	Address and command setup time, $^{t}IS_{b}$	-667 -53E -40E	20 25 35
33	Address and command hold time, $^{t}IH_{b}$	-667 -53E -40E	27 37 47
34	Data/data mask input setup time, $^{t}DS_{b}$	-667/-53E -40E	10 15
35	Data/data mask input hold time, $^{t}DH_{b}$	-667 -53E -40E	17 22 27
36	Write recovery time, ^{t}WR		3C
37	Write to read CMD delay, ^{t}WTR	-667/-53E -40E	1E 28
38	Read to precharge CMD delay, ^{t}RTP		1E
39	Memory analysis probe		00
40	Extension for bytes 41 and 42		00
41	MIN active auto refresh time, ^{t}RC	-667/-53E -40E	3C 37
42	MIN auto refresh to active/ auto refresh command period, ^{t}RFC		69
43	SDRAM device MAX cycle time, $^{t}CK_{MAX}$		80
44	SDRAM device MAX DQS–DQ skew time, $^{t}DQSQ$	-667 -53E -40E	18 1E 23
45	SDRAM device MAX read data hold skew factor, ^{t}QHS	-667 -53E -40E	22 28 2D
46	PLL relock time		0F
47–61	Optional features, not supported		00
62	SPD revision	Release 1.2	12
63	Checksum for bytes 0–62	-667 -53E -40E	8D/91 38/3C 9F/A3
64	Manufacturer's JEDEC ID code	MICRON	2C
65-71	Manufacturer's JEDEC ID code	(continued)	FF
72	Manufacturing location	01–12	01–0C
73-90	Module part number (ASCII)		Variable data
91	PCB identification code	1–9	01–09
92	Identification code (continued)	0	00
93	Year of manufacture in BCD		Variable data
94	Week of manufacture in BCD		Variable data
95-98	Module serial number		Variable data
99-127	Manufacturer-specific data (RSVD)		–

Notes: 1. The ^{t}RAS SPD value shown is based on the JEDEC standard value of 45ns; the actual device specification is ^{t}RAS = 40ns.

Module Dimensions

Figure 4: 240-Pin DDR2 DIMM



Notes:
1. All dimensions are in millimeters (inches).
2. The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

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